SLM27211 120-V, 4-A Peak, High-Frequency High-Side and Low-Side Driver

GENERAL DESCRIPTION

The SLM27211 is a high-frequency N-channel MOSFET driver include a 120V bootstrap diode and high-side and low-side drivers with independent inputs for maximum control flexibility. This allows for N-channel MOSFET control in half-bridge, full-bridge, two-switch forward, and active clamp forward converters. The low-side and the high-side gate drivers are independently controlled and matched to 2ns between the turn on and turn off of each other.

An on-chip bootstrap diode eliminates the external discrete diodes. Under voltage lockout is provided for both the high-side and the low-side drivers forcing the outputs low if the drive voltage is below the specified threshold.

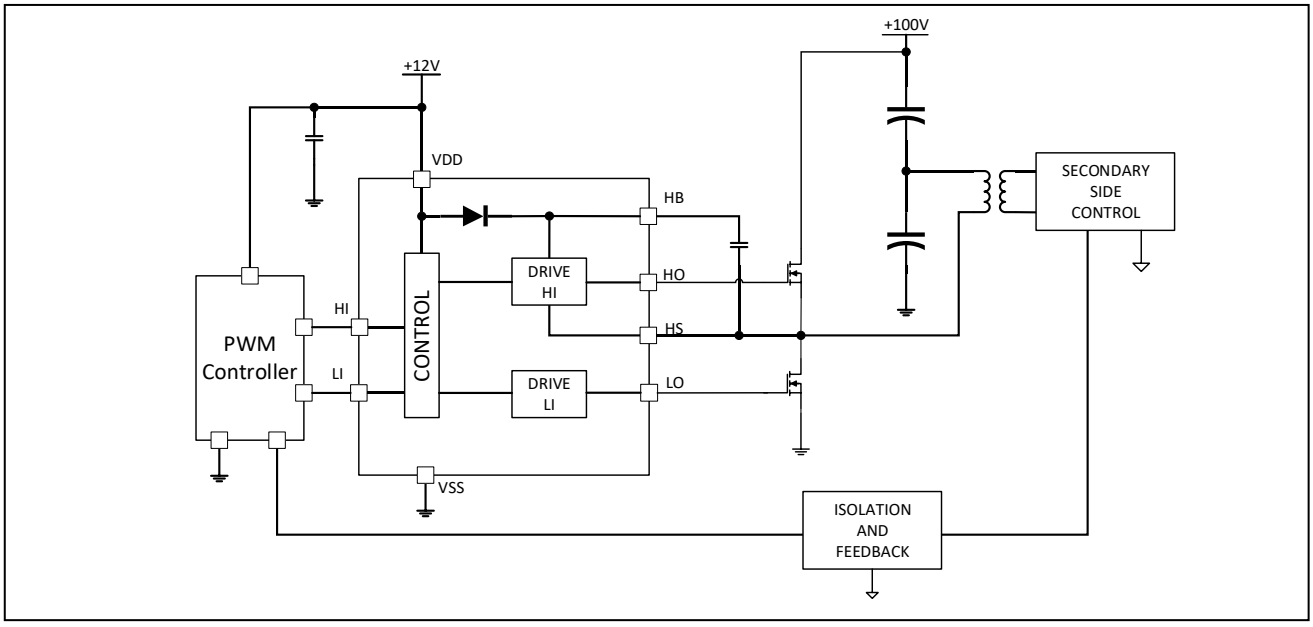
TYPICAL APPLICATIONS

- Power supplies for telecom, Datacom, and merchant
- Half-Bridge and Full-Bridge converters
- Push-Pull converters
- High voltage synchronous-buck converters
- Two-Switch forward converters
- Active-Clamp forward converters
- Class-D audio amplifiers

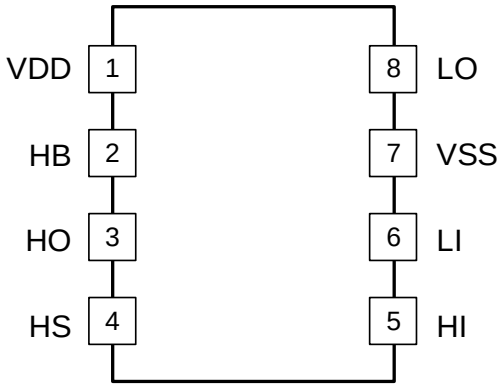
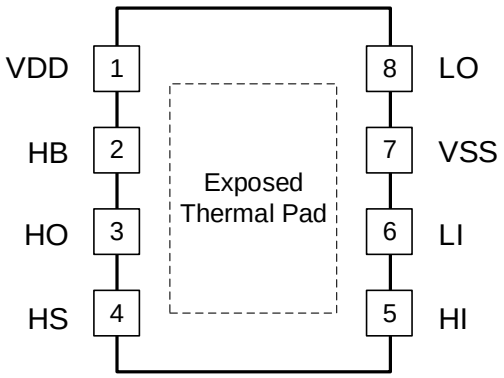
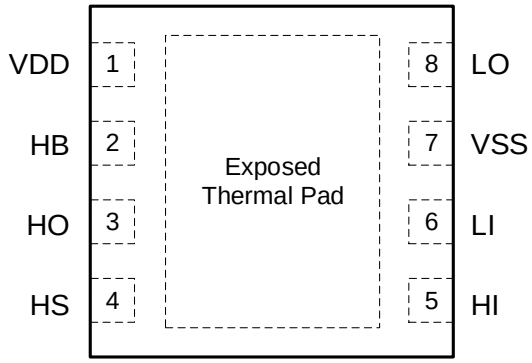
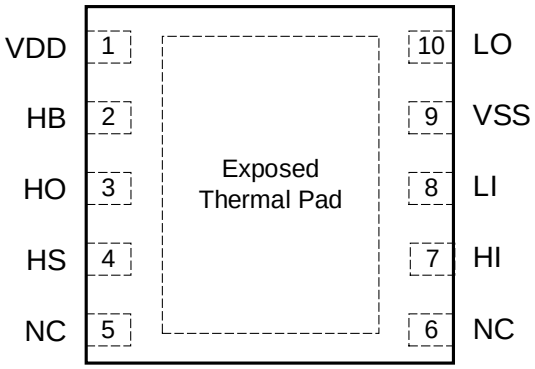
FEATURES

- Drives two N-Channel MOSFETs in high-side and low-side configuration
- Input pins are Independent of supply voltage range
- Maximum boot voltage of 120 V
- 8V to 17V VDD operation range
- 4.5A sink and 3A source output currents
- 7ns rise and 5ns fall time with1000pF load
- 22ns(typical) propagation delay time
- Under voltage lockout for high-side and low-side driver
- 2ns delay matching
- Package options: SOP8, SOP8-EP, DFN4x4-8, DFN4x4-10.

TYPICAL APPLICATION CIRCUIT



PIN CONFIGURATION

Package	Pin Configuration (Top View)	
SOP8/SOP8-EP		
DFN4x4-8		
DFN4x4-10		

PIN DESCRIPTION

No. SOP8, SOP8-EP, DFN4x4-8	Package DFN4x4-10	Name	Description
1	1	V_{DD}	Positive supply to the lower-gate driver. De-couple this pin to V_{SS} (GND). Typical decoupling capacitor range is 0.22 µF to 4.7 µF.
2	2	HB	High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022 µF to 0.1 µF. The capacitor value is dependent on the gate charge of the high-side MOSFET and must also be selected based on speed and ripple criteria.
3	3	HO	High-side output. Connect to the gate of the high-side power MOSFET.
4	4	HS	High-side source connection. Connect to source of high-side power MOSFET. Connect the negative side of bootstrap capacitor to this pin.
5	7	HI(1)	High-side input.
6	8	LI(1)	Low-side input.
7	9	VSS	Negative supply terminal for the device that is generally grounded.
8	10	LO	Low-side output. Connect to the gate of the low-side power MOSFET.
	5，6	NC	No connect.
		Thermal Pad(2)	Utilized on the SOP8-EP, DFN4x4-8 and DFN4x4-10package only. Electrically referenced to VSS (GND). Connect to a large thermal mass trace or ground plane to dramatically improve thermal performance.

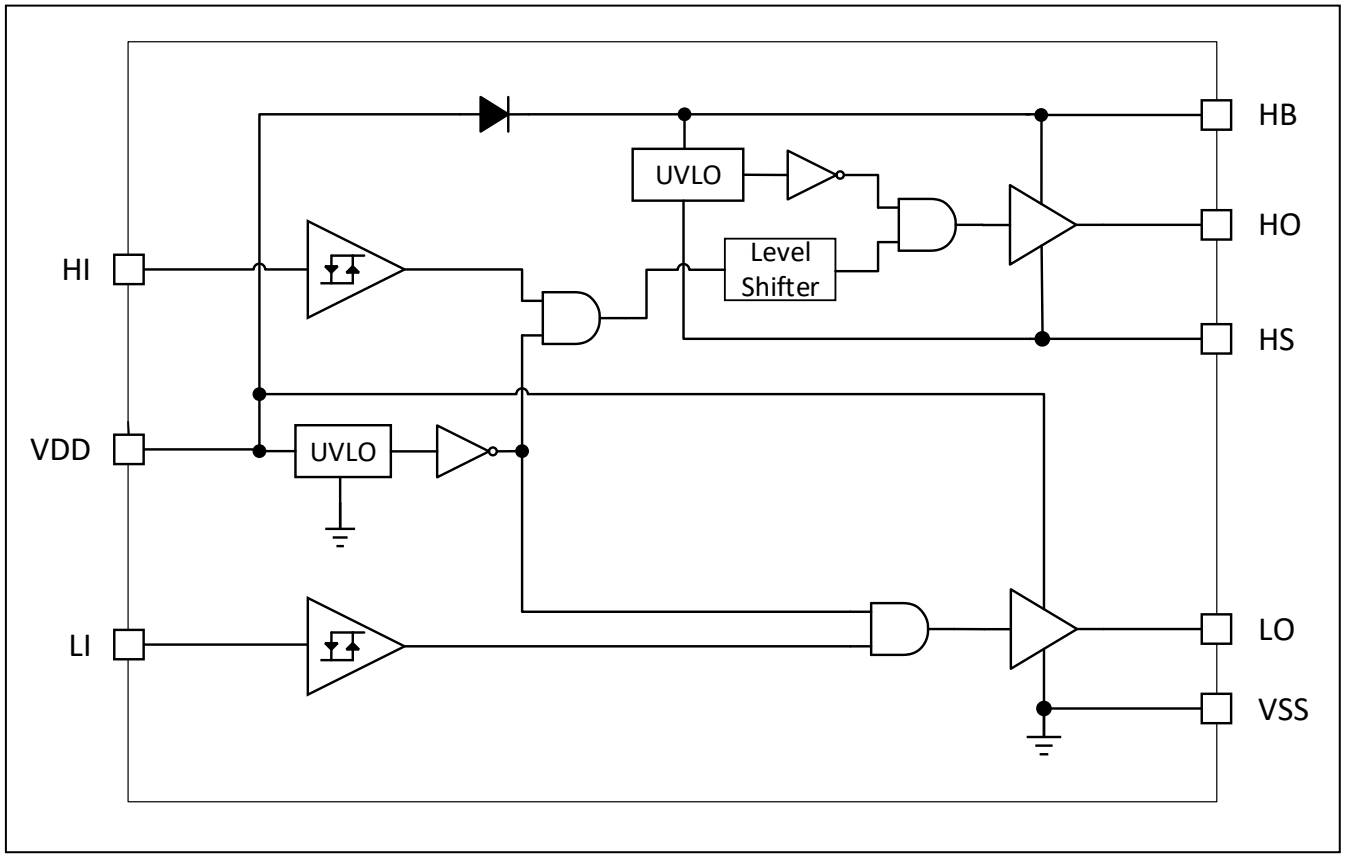
(1) HI or LI input is assumed to connect to a low impedance source signal. The source output impedance is assumed less than 100 Ω. If the source impedance is greater than 100 Ω, add a bypassing capacitor, each, between HI and VSS and between LI and VSS. The added capacitor value depends on the noise levels presented on the pins, typically from 1 nF to 10 nF should be effective to eliminate the possible noise effect. When noise is present on two pins, HI or LI, the effect is to cause HO and LO malfunctions to have wrong logic outputs.

(2) The thermal pad is not directly connected to any leads of the package; however, it is electrically and thermally connected to the substrate which is the ground of the device.

ORDERING INFORMATION

Order Part No.	Package	QTY
SLM27211CB-DG	SOP8-EP, Pb-Free	2500/Reel
SLM27211CA-DG	SOP8, Pb-Free	2500/Reel
SLM27211EK-DG	DFN4x4-8, Pb-Free	3000/Reel
SLM27211EL-7G	DFN4x4-10, Pb-Free	1000/Reel

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS(1)

		Min	Max	Unit
Supply voltage range, V_{DD}(2), V_{HB} – V_{HS}		-0.3	20	V
Input voltages on LI and HI, V_{LI}, V_{HI}		-0.3	20	V
Output voltage on LO, V_{LO}	DC	–0.3	V_{DD} + 0.3	V
	Repetitive pulse < 100 ns(3)	–2	V_{DD} + 0.3	
Output voltage on HO, V_{HO}	DC	V_{HS} – 0.3	V_{HB} + 0.3	V
	Repetitive pulse < 100 ns(3)	V_{HS} – 2	V_{HB} + 0.3	
Voltage on HS, V_{HS}	DC	–1	120	V
	Repetitive pulse < 100 ns(3)	–(24 V – VDD)	120	
Voltage on HB, V_{HB}		–0.3	120	V
Operating virtual junction temperature range, T_J		–40	150	°C
Storage temperature, T_{STG}		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to VSS unless otherwise noted. Currents are positive into and negative out of the specified terminal.

(3) Verified at bench characterization. VDD is the value used in an application design.

ESD RATINGS

Symbol	Definition	Value	Unit
V_{ESD}	HBM	±2000	V
	CDM	±1000	

THERMAL RESISTANCE

Package	θ_{JA}	Unit
SOP8	111.8	℃/W
SOP8-EP	41.1	℃/W
DFN4x4-8	37.7	℃/W
DFN4x4-10	50	℃/W

RECOMMENDED OPERATION CONDITIONS

All voltages are with respect to V_{SS}; currents are positive into and negative out of the specified terminal.

Symbol	Definition	Min	Nom	Max	Unit
V_{DD}	Supply voltage range on VDD	8	12	17	V
V_{BS}	Voltage between HB and HS	8	12	17	V
V_{HS}	Voltage on HS	–1		105	V
	Voltage on HS, V_{HS} (repetitive pulse < 100 ns)	–(24 V – VDD)		110	V
V_{HB}	Voltage on HB	V_{HS} + 8, V_{DD} – 1		V_{HS} + 17, 115	V
	Voltage slew rate on HS			50	V/ns
T_J	Operating junction temperature	–40		125	°C

STATIC ELECTRICAL CHARACTERISTICS

V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, no load on LO or HO, T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
SUPPLY CURRENTS						
I_{DD}	V_{DD} quiescent current	V(LI) = V(HI) = 0 V	0.08	0.115	0.15	mA
I_{DDO}	V_{DD} operation current	f = 500 kHz, C_{LOAD} = 0	0.7	1.0	1.5	mA
I_{HB}	Boot voltage quiescent current	V(LI) = V(HI) = 0 V	0.07	0.095	0.12	mA
I_{HBO}	Boot voltage operating current	f = 500 kHz, C_{LOAD} = 0	0.7	0.96	1.2	mA
I_{HBS}	HB to V_{SS} quiescent current	V(HS) = V(HB) = 115 V		0.02	1	µA
I_{HBSO}	HB to V_{SS} operating current	f = 500 kHz, C_{LOAD} = 0		0.15	0.5	mA
INPUT						
V_{HIT}	Input voltage threshold		1.9	2.3	2.6	V
V_{LIT}	Input voltage threshold		1.3	1.6	1.9	V
V_{IHYS}	Input voltage hysteresis			700		mV
R_{IN}	Input pulldown resistance			55		kΩ
UNDER-VOLTAGE LOCKOUT (UVLO)						
V_{DDR}	V_{DD} turn on threshold		6.4	7	7.7	V
V_{DDHYS}	Hysteresis			0.5		V
V_{HBR}	V_{HB} turn on threshold		5.7	6.7	7.7	V
V_{HBHYS}	Hysteresis			1.1		V
BOOTSTRAP DIODE						
V_F	Low-current forward voltage	I_{VDD-HB} = 100 µA		0.4	0.7	V
V_{FI}	High-current forward voltage	I_{VDD-HB} = 100 mA		0.82	0.95	V
R_D	Dynamic resistance, ΔVF/ΔI	I_{VDD-HB} = 100 mA and 80 mA	0.8	1.0	1.2	Ω
LO GATE DRIVER						
V_{LOL}	Low-level output voltage	I_{LO} = 100 mA	0.04	0.08	0.18	V
V_{LOH}	High level output voltage	I_{LO} = –100 mA, V_{LOH} = V_{DD} – V_{LO}	0.12	0.18	0.25	V
I_{SRC_L}	Peak pull-up current(1)	V_{LO} = 0 V		3		A
I_{SNK_L}	Peak pull-down current(1)	V_{LO} = 12 V		4.5		A
HO GATE DRIVER						
V_{HOL}	Low-level output voltage	I_{HO} = 100 mA	0.04	0.08	0.18	V
V_{HOH}	High-level output voltage	I_{HO} = –100 mA, V_{HOH} = V_{HB} – V_{HO}	0.12	0.18	0.25	V
I_{SRC_H}	Peak pull-up current(1)	V_{HO} = 0 V		3		A
I_{SNK_H}	Peak pull-down current(1)	V_{HO} = 12 V		4.5		A

(1) Ensured by design.

SWITCHING CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
T_{DLFF}	V_{LI} falling to V_{LO} falling	C_{LOAD} = 0	18	22	30	ns
T_{DHFF}	V_{HI} falling to V_{HO} falling		18	22	30	ns
T_{DLRR}	V_{LI} rising to V_{LO} rising		17	21	29	ns
T_{DHRR}	V_{HI} rising to V_{HO} rising		17	21	29	ns
T_{MON}	From HO OFF to LO ON			2	7	ns
T_{MOFF}	From LO OFF to HO ON			2	7	ns
t_R	LO rise time	C_{LOAD} = 1000 pF, from 10% to 90%		7		ns
t_R	HO rise time			7		ns
t_F	LO fall time	C_{LOAD} = 1000 pF, from 90% to 10%		5		ns
t_F	HO fall time			5		ns
t_R	LO, HO	C_{LOAD} = 0.1 µF, (3 V to 9 V)		0.35	0.5	µs
t_F	LO, HO	C_{LOAD} = 0.1 µF, (9 V to 3 V)		0.16	0.3	µs
Minimum input pulse width that changes the output					50	ns
Bootstrap diode turn off time (1)(2)		I_F = 20 mA, I_{REV} = 0.5 A(3)		20		ns

(1) Ensured by design.

(2) I_F: Forward current applied to bootstrap diode, I_{REV}: Reverse current applied to bootstrap diode.

(3) Typical values for T_A = 25°C.

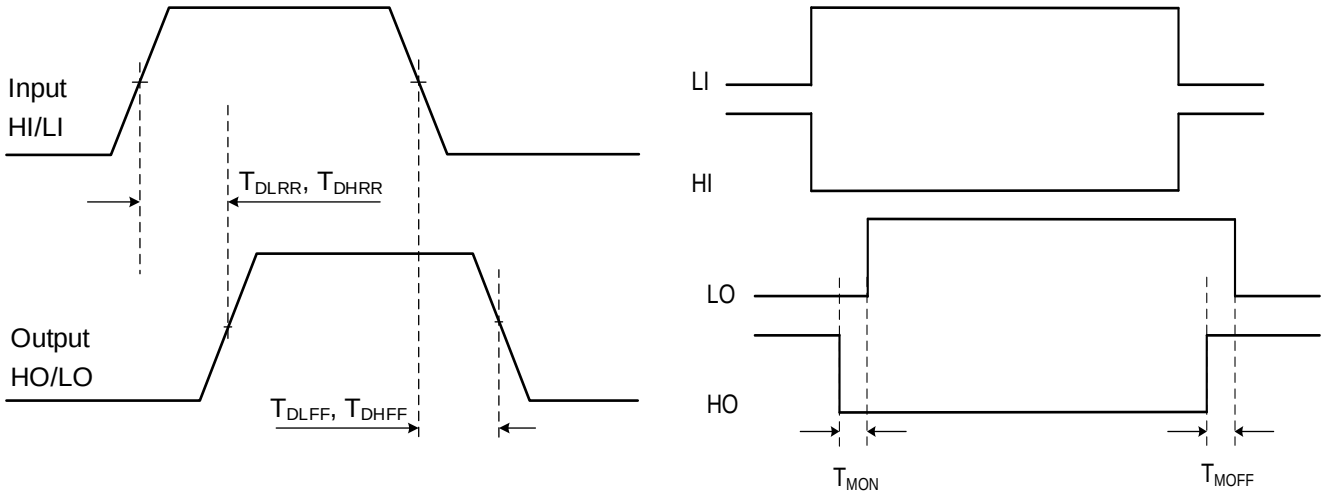


Figure 1. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

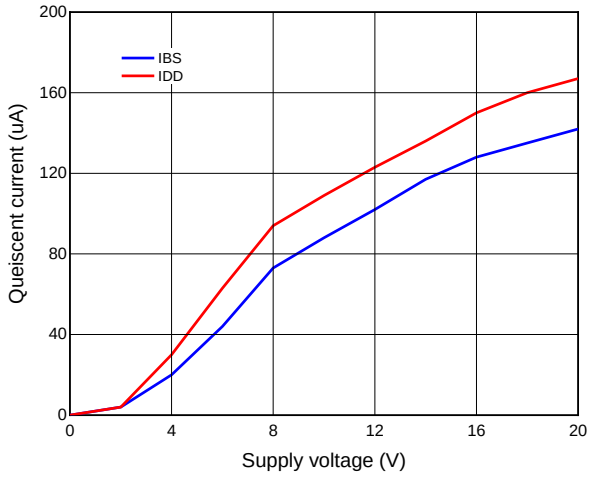


Figure 2. Quiescent Current vs. Supply Voltage

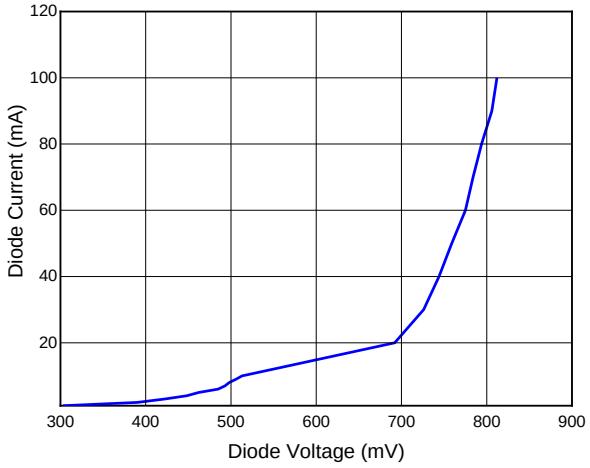


Figure 3. Diode Current vs Diode Voltage

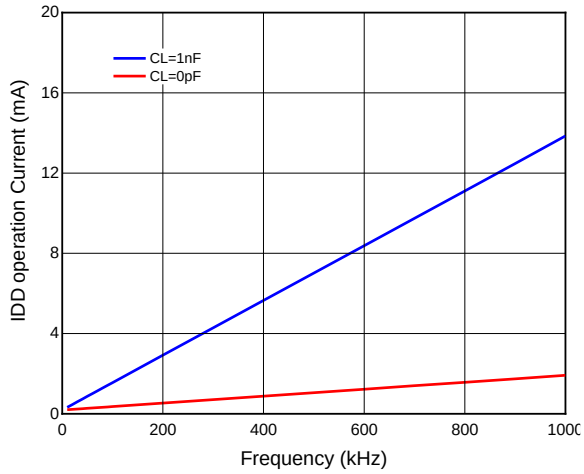


Figure 4. IDD Operation Current vs. Frequency

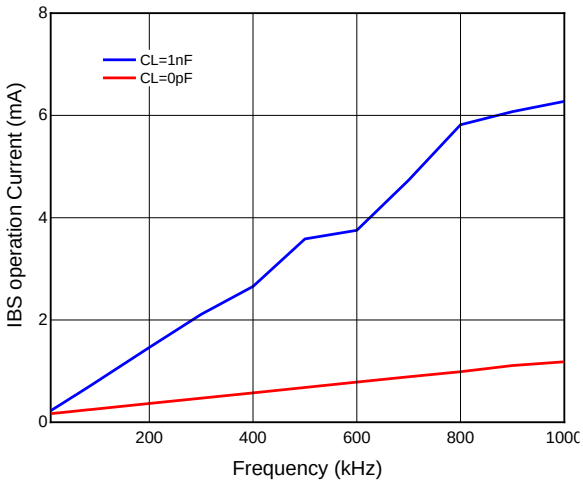


Figure 5. Boot Voltage Operation Current vs Frequency

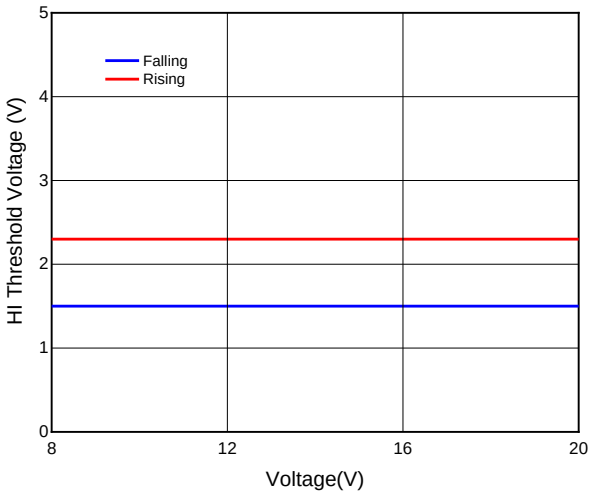


Figure 6. High Side Input Threshold vs Supply Voltage

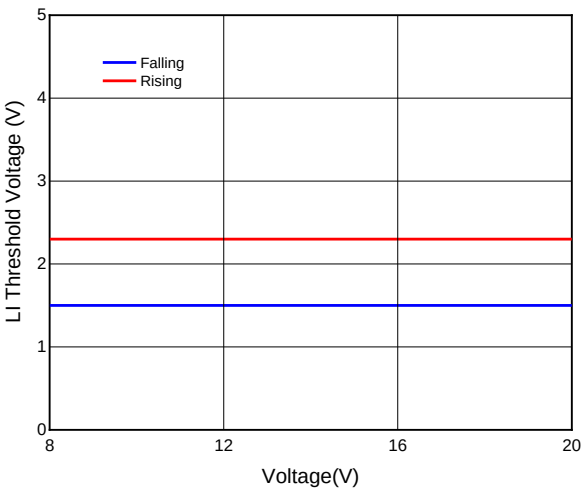


Figure 7. Low Side Input Threshold vs Supply Voltage

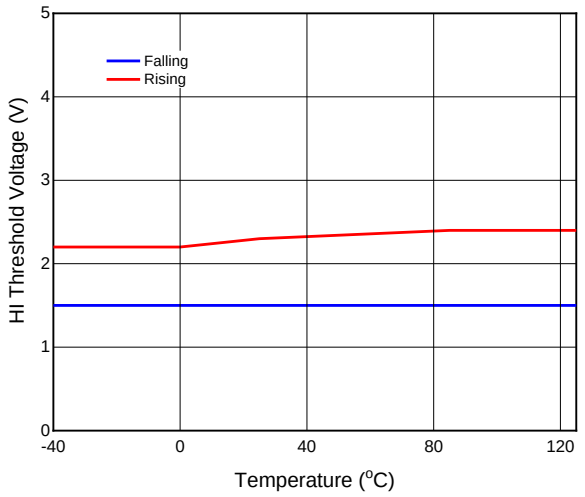


Figure 8. High Side Input Threshold vs Temperature

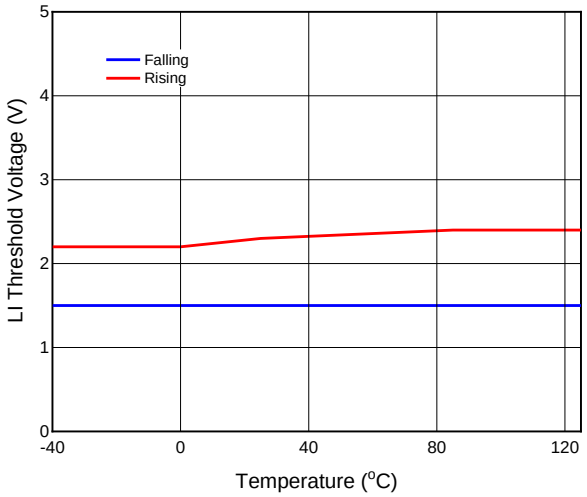


Figure 9. Low Side Input Threshold vs Temperature

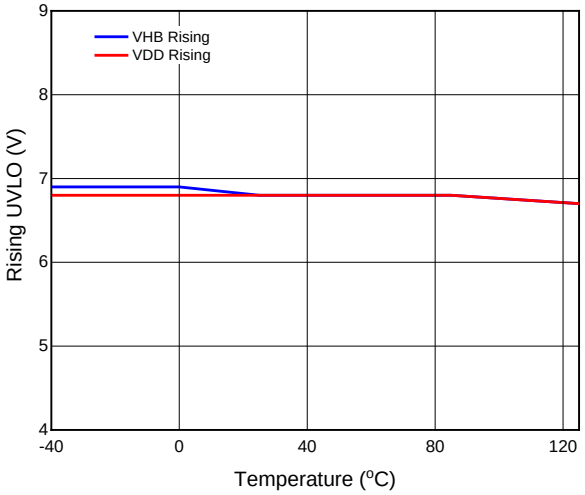


Figure 10. Rising Threshold Voltage vs Temperature

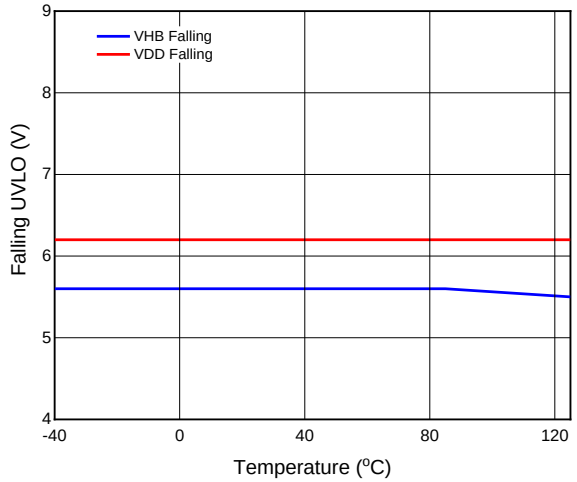


Figure 11. Falling Threshold Voltage vs Temperature

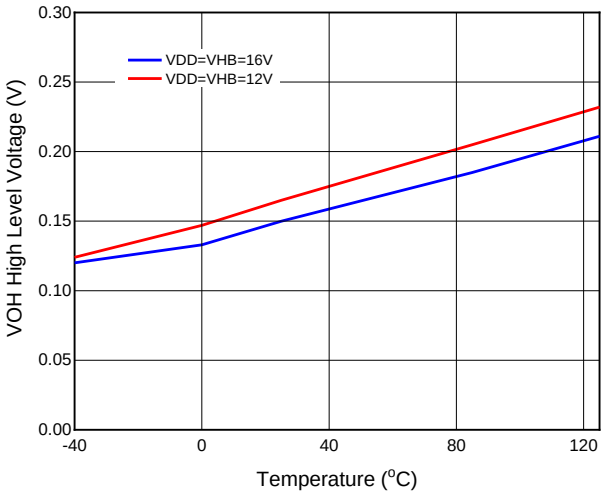


Figure 12. HO High Level Output Voltage vs Temperature

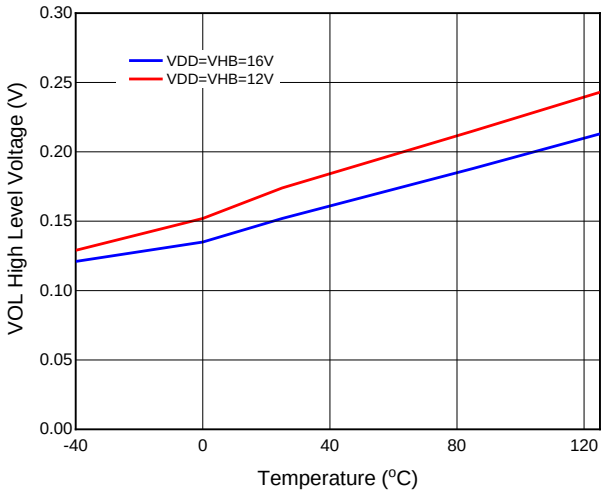


Figure 13. LO High Level Output Voltage vs Temperature

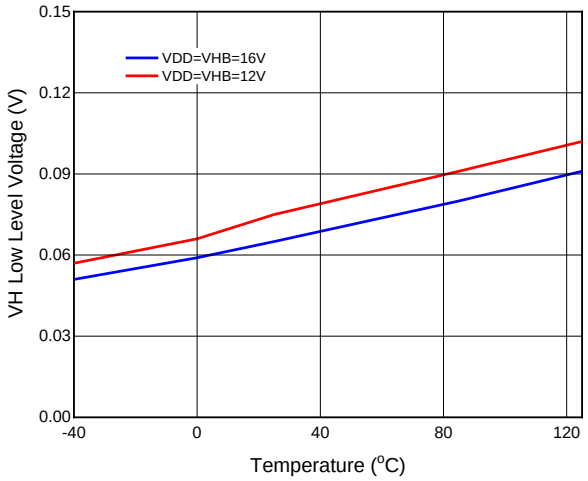


Figure 14. HO Low Level Output Voltage vs Temperature

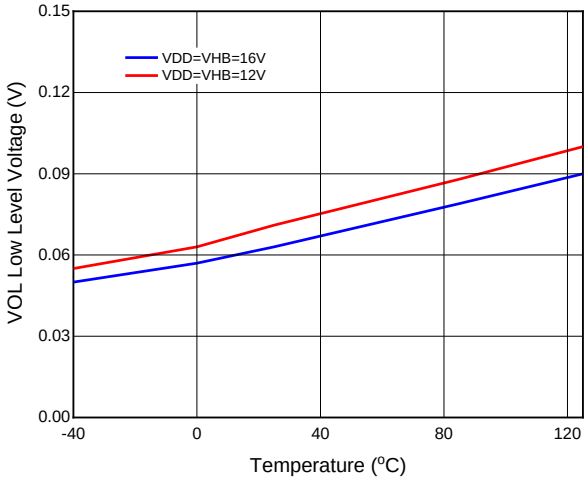


Figure 15. LO Low Level Output Voltage vs Temperature

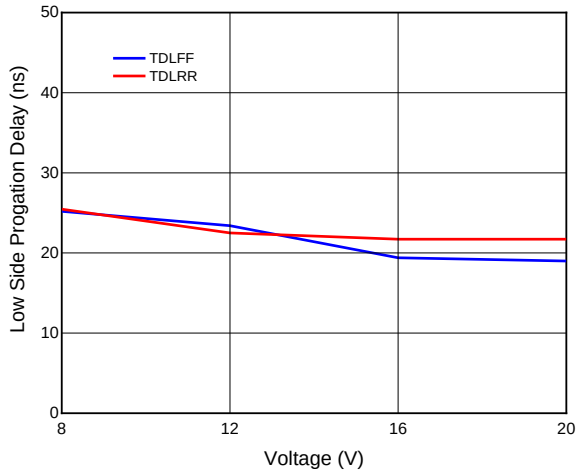


Figure 16. Low Side Propagation Delay vs Voltage

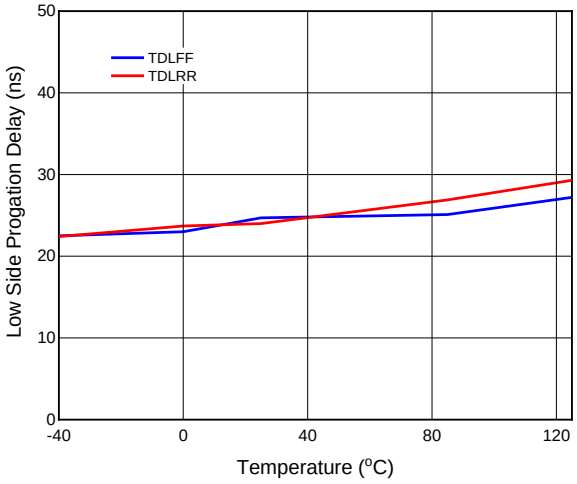


Figure 17. Low Side Propagation Delay vs Temperature

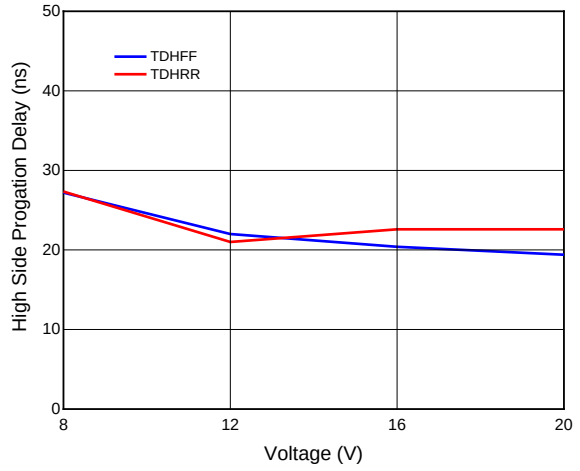


Figure 18. High Side Propagation Delay vs Voltage

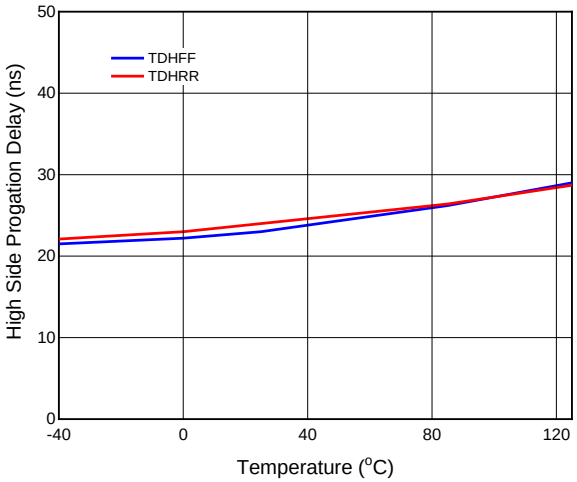


Figure 19. High Side Propagation Delay vs Temperature

DEVICE FUNCTIONAL MODES

The device operates in normal mode and UVLO mode. In the UVLO mode, the output (HO and LO) both hold low. In the normal mode the output state is dependent on states of the HI and LI pins. Table 2 lists the output states for different input pin combinations.

Table 2. Device Logic Table

HI PIN	LI PIN	HO(1)	LO(2)
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H

(1) HO is measured with respect to HS.

(2) LO is measured with respect to VSS.

APPLICATION INFORMATION

To affect fast switching of power devices and reduce associated switching power losses, a powerful gate driver is employed between the PWM output of controllers and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation will be often encountered because the PWM signal from the digital controller is often a 3.3V logic signal which cannot effectively turn on a power switch. Level shifting circuitry is needed to boost the 3.3V signal to the gate drive voltage (such as 12 V) in order to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN/PNP bipolar transistors in totem-pole arrangement, being emitter follower configurations, prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers, and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

POWER DISSIPATION

Power dissipation of the gate driver has two portions as shown in Equation 1.

$$P_{DISS} = P_{DC} + P_{SW} \quad (1)$$

The DC portion of the power dissipation is $P_{DC} = I_Q \times VDD$ where I_Q is the quiescent current for the driver. The quiescent current is the current consumed by the device to bias all internal circuits such as input stage, reference voltage, logic circuits, protections, and also any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through, and so forth). The SLM27211 features very low quiescent currents and contain internal logic to eliminate any shoot-through in the output driver stage. Thus, the effect of the P_{DC} on the total power dissipation within the gate driver can be safely assumed to be negligible. The power dissipated in the gate-driver package during switching (P_{SW}) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage VG, which is very close to input bias supply voltage V_{DD})
- Switching frequency
- Use of external gate resistors. When a driver device is tested with a discrete, capacitive load calculating the power that is required from the bias supply is fairly simple. The energy that must be transferred from the bias supply to charge the capacitor is given by Equation 2.

$$EG = ½ \times C_{LOAD} \times V_{DD}^2 \quad (2)$$

Here, C_{LOAD} is load capacitor and V_{DD} is bias voltage feeding the driver

There is an equal amount of energy dissipated when the capacitor is charged and when it is discharged. This leads to a total power loss given by Equation 3.

$$PG = C_{LOAD} \times V_{DD}^{2} \times f_{SW} \quad (3)$$

Here, f_{SW} is the switching frequency

The switching load presented by a power MOSFET/IGBT is converted to an equivalent capacitance by examining the gate charge required to switch the device. This gate charge includes the effects of the input capacitance plus the added charge needed to swing the drain voltage of the power device as it switches between the ON and OFF states. Most manufacturers provide specifications of typical and maximum gate charge, in nC, to switch the device under specified conditions. Using the gate charge Qg, determine the power that must be dissipated when switching a capacitor which is calculated using the equation $Q_G = C_{LOAD} \times V_{DD}$ to provide Equation 4 for power.

$$P_G = C_{LOAD} \times V_{DD}^2 \times f_{SW} = Q_G \times V_{DD} \times f_{SW} \quad (4)$$

This power P_G is dissipated in the resistive elements of the circuit when the MOSFET/IGBT is being turned on and off. Half of the total power is dissipated when the load capacitor is charged during turn on, and the other half is dissipated when the load capacitor is discharged during turn off. When no external gate resistor is employed between the driver and MOSFET/IGBT, this power is completely dissipated inside the driver package. With the use of external gate-drive resistors, the power dissipation is shared between the internal resistance of driver and external gate resistor.

POWER SUPPLY RECOMMENDATIONS

The bias supply voltage range for which the SLM27211 device is recommended to operate is from 8 V to 17 V. The lower end of this range is governed by the internal under voltage-lockout (UVLO) protection feature on the V_{DD} pin supply circuit blocks. Whenever the driver is in UVLO condition when the VDD pin voltage is below the supply start threshold (V_{DDR}), this feature holds the output low, regardless of the status of the inputs. The upper end of this range is driven by the 20V absolute maximum voltage rating of the VDD pin of the device (which is a stress rating). Keeping a 3V margin to allow for transient voltage spikes, the maximum recommended voltage for the V_{DD} pin is 17 V. The UVLO protection feature also involves a hysteresis function, which means that when the V_{DD} pin bias voltage has exceeded the threshold voltage and device begins to operate, and if the voltage drops, then the device continues to deliver normal functionality unless the voltage drop exceeds the hysteresis specification V_{DDHYS}. Therefore, ensuring that, while operating at or near the 8V range, the voltage ripple on the auxiliary power supply output is smaller than the hysteresis specification of the device is important to avoid triggering device shutdown. During system shutdown, the device operation continues until the V_{DD} pin voltage has dropped below (V_{DDR}-V_{DDHYS}), which must be accounted for while evaluating system shutdown timing design requirements. Likewise, at system start-up the device does not begin operation until the V_{DD} pin voltage has exceeded the V_{DDR} threshold.

The quiescent current consumed by the internal circuit blocks of the device is supplied through the VDD pin. Although this fact is well known, it is important to recognize that the charge for source current pulses delivered by the LO pin is also supplied through the same VDD pin. As a result, every time a current is sourced out of the LO pin, a corresponding current pulse is delivered into the device through the VDD pin. Thus, ensure that a local bypass capacitor is provided between the VDD and VSS pin and located as close to the device as possible for the purpose of decoupling. A low-ESR, ceramic surface-mount capacitor is required. Sillumin recommends using a capacitor in the range 0.22 µF to 4.7 µF between VDD and VSS. In a similar manner, the current pulses delivered by the HO pin are sourced from the HB pin. Therefore, a local decoupling capacitor is needed between the HB and HS pins and its value depends on the external MOSFET or IGBT used and the switching frequency.

TYPICAL APPLICATION

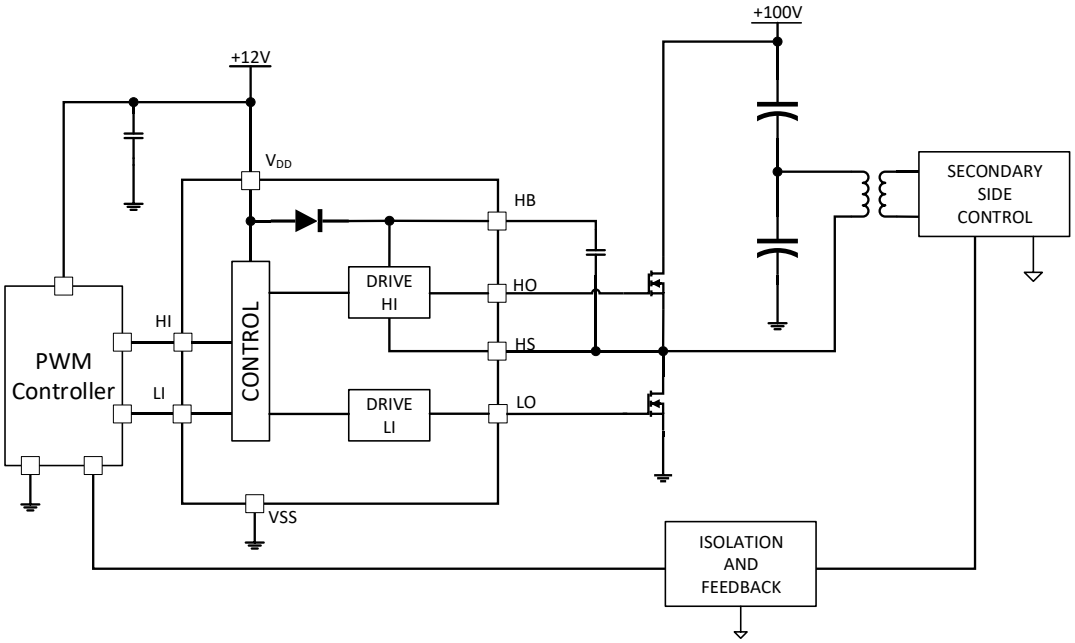


Figure 20. SLM27211 Typical Application Circuit in Half Bridge

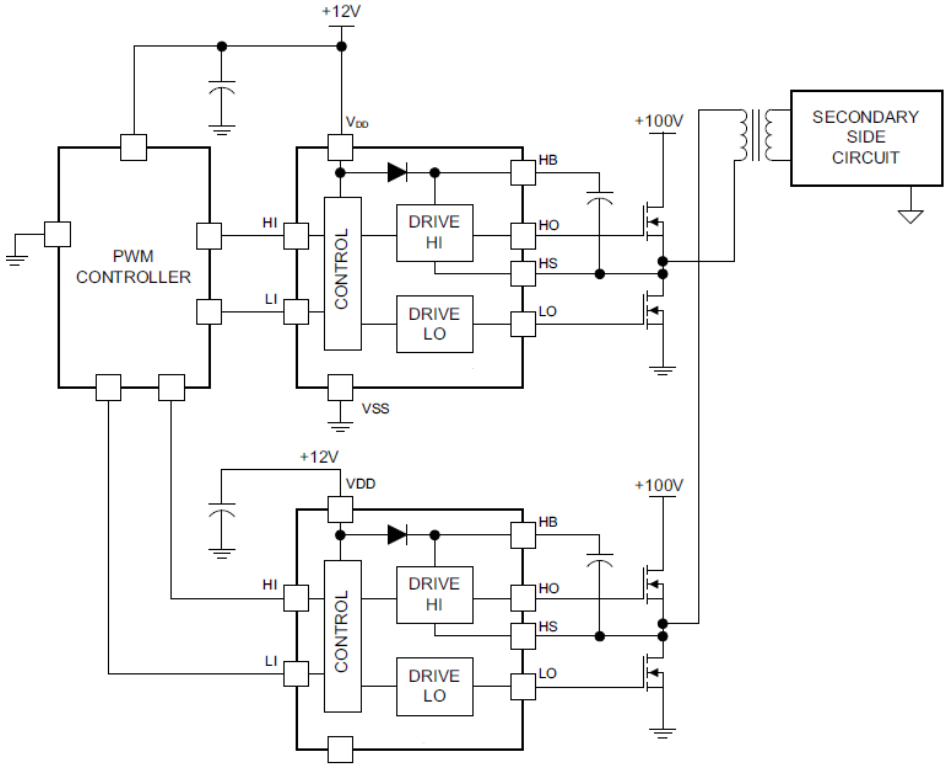
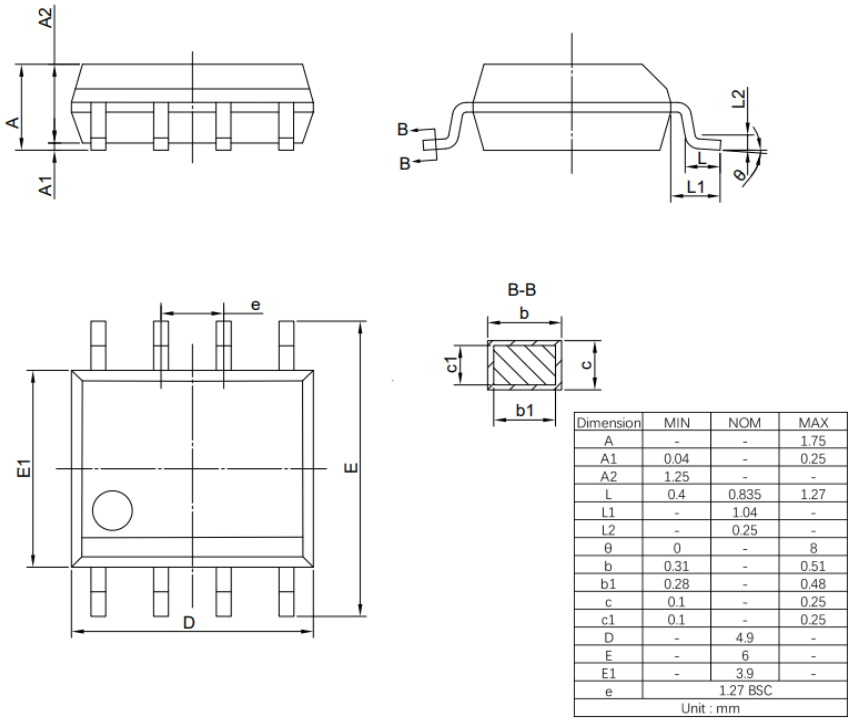


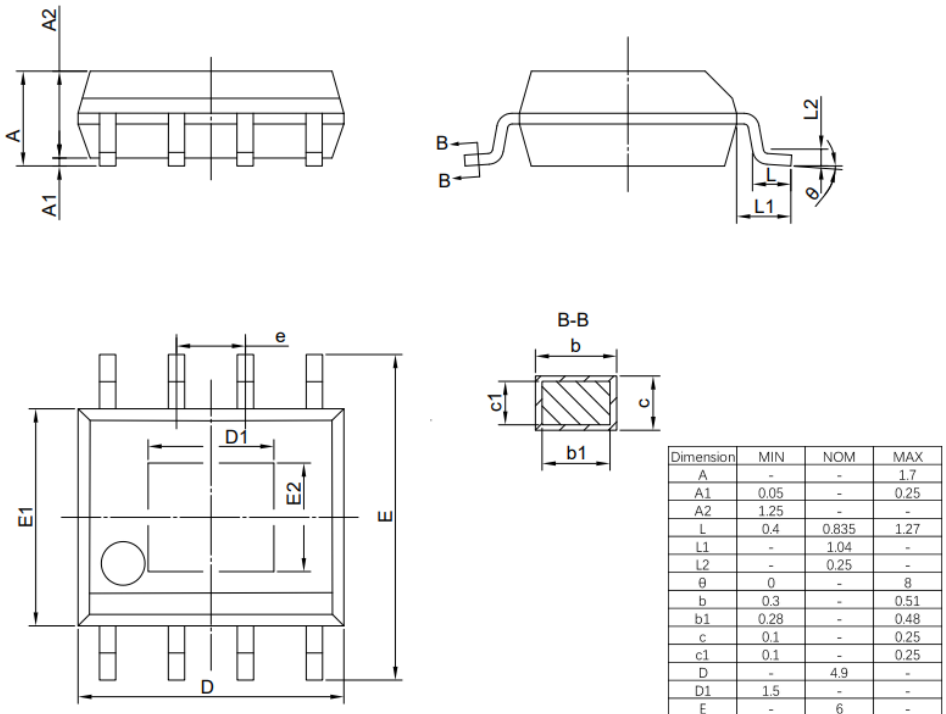
Figure 21. SLM27211 Typical Application Circuit in Full Bridge

PACKAGE CASE OUTLINES



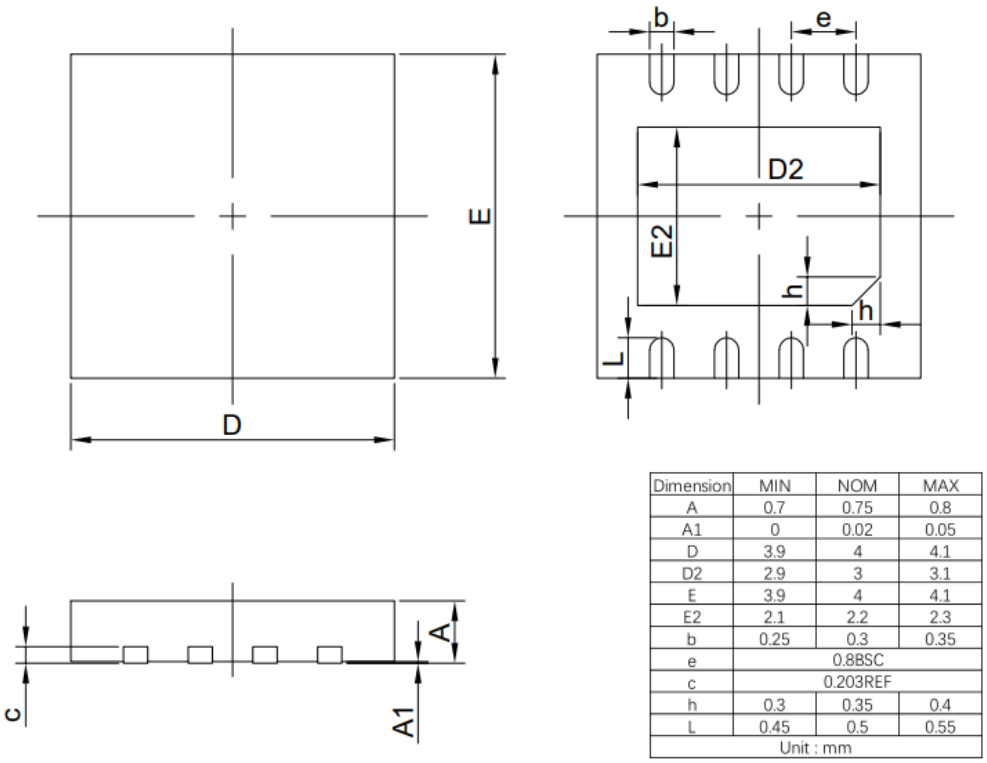
Dimension	MIN	NOM	MAX
A	-	-	1.75
A1	0.04	-	0.25
A2	1.25	-	-
L	0.4	0.835	1.27
L1	-	1.04	-
L2	-	0.25	-
θ	0	-	8
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.1	-	0.25
c1	0.1	-	0.25
D	-	4.9	-
E	-	6	-
E1	-	3.9	-
e	1.27 BSC		
Unit : mm			

Figure 22. SOP8 Outline Dimensions



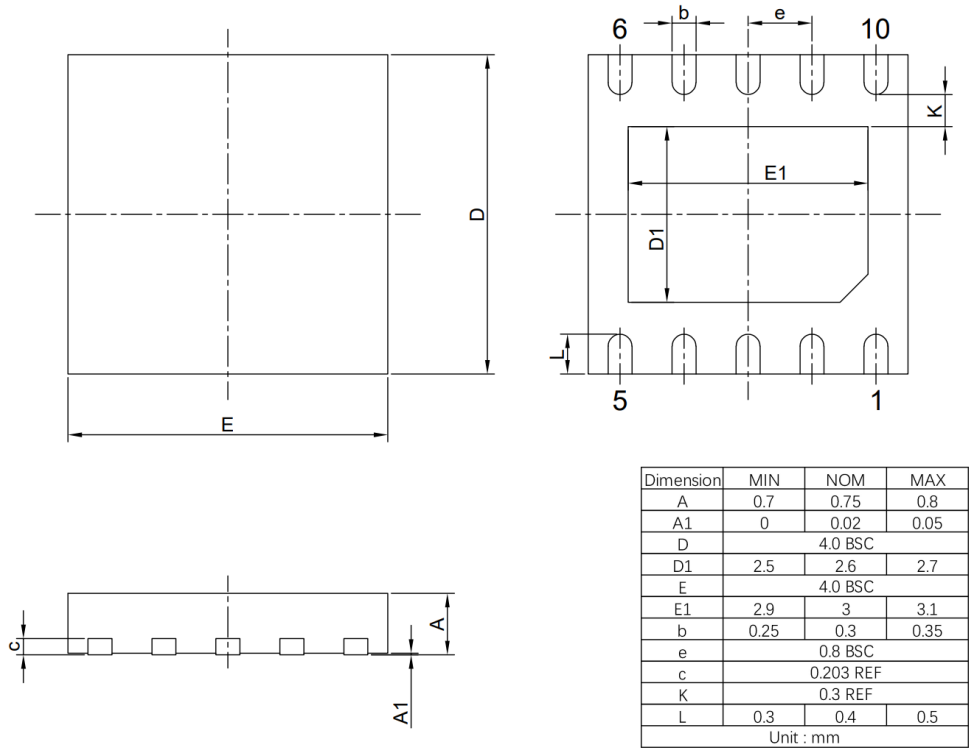
Dimension	MIN	NOM	MAX
A	-	-	1.7
A1	0.05	-	0.25
A2	1.25	-	-
L	0.4	0.835	1.27
L1	-	1.04	-
L2	-	0.25	-
θ	0	-	8
b	0.3	-	0.51
b1	0.28	-	0.48
c	0.1	-	0.25
c1	0.1	-	0.25
D	-	4.9	-
D1	1.5	-	-
E	-	6	-
E1	-	3.9	-
E2	1	-	-
e	1.27 BSC		
Unit : mm			

Figure 23. SOP8-EP Outline Dimensions



Dimension	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
D	3.9	4	4.1
D2	2.9	3	3.1
E	3.9	4	4.1
E2	2.1	2.2	2.3
b	0.25	0.3	0.35
e	0.8BSC		
c	0.203REF		
h	0.3	0.35	0.4
L	0.45	0.5	0.55
Unit : mm			

Figure 24. DFN4x4-8 Outline Dimensions



Dimension	MIN	NOM	MAX
A	0.7	0.75	0.8
A1	0	0.02	0.05
D	4.0 BSC		
D1	2.5	2.6	2.7
E	4.0 BSC		
E1	2.9	3	3.1
b	0.25	0.3	0.35
e	0.8 BSC		
c	0.203 REF		
K	0.3 REF		
L	0.3	0.4	0.5
Unit : mm			

Figure 25. DFN4x4-10 Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 Datasheet, 2022-05-05	
Whole document	Initial released
Rev 1.1 Datasheet, 2023-02-05	
Update Package Case Outlines	Add DFN4x4-10 package
Rev 1.2 Datasheet, 2023-02-20	
Update Thermal Resistance	Add DFN4x4-10 thermal resistance
Rev 1.3 Datasheet, 2023-04-13	
Page 2,3	Update DFN4x4-10 pin configuration and Order Information